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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,406	10/29/2003	Russell W. Guenthner	52003218	7204

7590 05/31/2005

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13430 North Black Canyon Highway
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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,406	GUENTHNER ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/697,406 filed on 10/29/2003. Claims 1-4 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Rahut et al. (6,766,504).

4. As to claim 1, Rahut et al. teach a method for optimizing the timing performance of an overall logic circuit implemented in a FPGA (see col. 1) with programmable interconnect behaving in a way that timing of logic signals routed by the programmable interconnect from a specific source to a specific load with the FPGA is affected negligibly by fanout to other logic loads connected to the same source signal (Fig. 1 shown part of the circuit implemented; Fig. 2-3 shown the method for optimizing the timing) comprising a) synthesizing the overall logic for the first implementation in an FPGA including construction and first placement of the logic functions on the FPGA (Fig. 1); b) analyzing the timing (timing information; routing in delay mode; col. 4 lines

23-37); c) determining the most critical timing paths (at least the reference teaches routing only one more critical connections of a selected logic level until reaching destination by disregarding other connections or other loads; col. 4, lines 23-37; Fig. 1A-1C, thick line of connections are example of most critical path, disregarding non-critical thin line connections); d) selecting as an object for implementing a specific critical path (at least the reference teaches routing only one more critical connections of a selected logic level until reaching destination by disregarding other connections or other loads; col. 4, lines 23-37); e) implementing in another way the critical logic in the chosen critical path with implementation of the critical logic performed with relative disregard as to the fanout of signals to other logic in the overall logic circuit and with placement of logic in the chosen critical path designed primarily to minimize the interconnected routing distance of the signal contributing to that chosen critical path (at least the reference teaches routing only one more critical connections of a selected logic level until reaching destination by disregarding other connections or other loads; col. 4, lines 23-37) (see also summary, Fig. 1-3 and its description for detailed information).

5. As to claims 2 and 4, Rahut et al. also teach the implementation of the critical logic in a new way in step e) is limited only to changes in the placement of the logic in the chosen critical path (routing only one more critical connections of a selected logic level until reaching destination by disregarding other connections or other loads; col. 4, lines 23-37) (see also summary, Fig. 1-3 and its description for detailed information).

6. As to claim 3, Rahut et al. teach a method for optimizing the timing performance of an overall logic circuit implemented in a FPGA (see col. 1) with programmable

interconnect behaving in a way that timing of logic signals routed by the programmable interconnect from a specific source to a specific load with the FPGA is affected negligibly by fanout to other logic loads connected to the same source signal (Fig. 1 shown part of the circuit implemented; Fig. 2-3 shown the method for optimizing the timing) comprising a) synthesizing the overall logic for the first implementation in an FPGA including construction and first placement of the logic functions on the FPGA (Fig. 1); b) analyzing the timing (timing information; routing in delay mode; col. 4 lines 23-37); c) determining the most critical timing paths (at least the reference teaches routing only one more critical connections of a selected logic level until reaching destination by disregarding other connections or other loads; col. 4, lines 23-37; Fig. 1A-1C, thick line of connections are example of most critical path, disregarding non-critical thin line connections); d) selecting as an object for implementing a specific critical path (at least the reference teaches routing only one more critical connections of a selected logic level until reaching destination by disregarding other connections or other loads; col. 4, lines 23-37); e) implementing in another way the critical logic in the chosen critical path with implementation of the critical logic performed with relative disregard as to the fanout of signals to other logic in the overall logic circuit and with placement of logic in the chosen critical path designed primarily to minimize the interconnected routing distance of the signal contributing to that chosen critical path (at least the reference teaches routing only one more critical connections of a selected logic level until reaching destination by disregarding other connections or other loads; col. 4, lines 23-37); f) modifying the placement of other logic in the overall logic circuit in

accommodate the changes in placement of the chosen critical path while maintaining approximately the new placement of the critical logic and g) repeating the step b) through f) where the last implementation and placement of the overall logic circuit from step f) becomes the basis for starting again with this last implementation becoming the base implementation (at least the reference teaches routing only one more critical connections of a selected logic level until reaching destination by disregarding other connections or other loads; col. 4, lines 23-37) (see also summary, Fig. 1-3 and its description for detailed information).

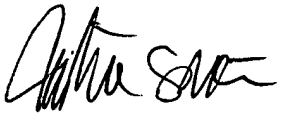
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek



VUTHE SIEK
PRIMARY EXAMINER